Poornima University, Jaipur

Sponsored Project

Numerical Simulation and Compact Modelling of Organic Thin Film Transistors (OTFTs) for Future Flexible Electronics

- **Introduction of the Sponsored Project -:**

Dr Arun Dev Dhar Dwivedi, Professor Department of Electrical and Electronics Engineering, Poornima University Jaipur has been awarded by Early Career Research Award by Science and Engineering Research Board (SERB), Department of Science and Technology (DST) government of India and a project entitled "Numerical Simulation and Compact modeling of Organic Thin Film Transistors (OTFTs) for Future Flexible Electronics" of total cost Rs 5000000.00 has been approved under this scheme.
Dr. Arun Dev Dhar Dwivedi
Winner of Early Career Research Award & Grant of INR 5 Million
by Science and Engineering Research Board & Department of Science & Technology.
Approval Letter

File Number: ECR/2017/000179

Dated: 03-Apr-2017

Subject: Project titled "Numerical Simulation and Compact modeling of Organic Thin Film Transistors (OTFTs) for Future Flexible Electronics".

Dear Dr. Arundevdhar Dwivedi,

The project cited above has been approved by Science and Engineering Research Board (SERB) for funding, subject to fulfilling the eligibility criteria, please visit our website www.serb.gov.in, www.serbonline.in for the terms & conditions of the grant. The following are the approved items for a period of 3 years. The final budget to be sanctioned would be based on quotations received, existing norms etc.

The committee recommended the following budget

Manpower:
-> JRF - 1

Equipment Details:
-> vacuum coating unit, TCAD, EDA, Semiconductor Parameter Analyzer, computer and printer - 1

Consumables: Rs. 150000

Travel Cost: As per norms

Contingencies: As per norms

Overhead: As per norms

Kindly follow the below steps only then you will be able to acknowledge the approval letter:

1. Go to www.serbonline.in through your credentials
2. Go to Menu --> Proposal submission --> View submitted proposals
3. Click on the link under Status column "Proposal Approved, Acknowledgment pending from PI"

You are requested to upload the lowest quotation for above equipment within the approved budget preferably within 15 days of the receipt of this letter in order to process the project for the release of funds. In case, we do not receive the above information within ONE MONTH of the issue of this approval letter, it would be presumed that you are not interested in this project and the offer would automatically stand withdrawn. No further correspondence will be entertained thereafter. A certificate stating that any visit abroad for a period more than eight weeks would be undertaken after due permission from SERB, may also be submitted.

Kindly upload RTGS details of the implementing institute to facilitate transfer of the fund as per the template. Kindly quote the reference number in all future correspondence. The project's reference no. ECR/2017/000179 may also be mentioned in all research communications arising from the above project.

(Dr. Ramesh Vijayan)

SCIENTIST-C
• **Details of Research Project –**

**Project Summary:** Since organic materials can be deposited at lower temperature, they provide a strong compatibility with the flexible substrates including plastic, paper, fiber, foil, and even smart cloth in comparison to their inorganic counterparts. OTFT, the most prominent device among the organic devices, is now exhibiting much higher or comparable performance to hydrogenated amorphous silicon TFTs (a-Si:H TFTs) commonly used as the pixel drivers in active matrix flat-panel displays (AMFPDs). These additional degrees of freedom for the OTFTs raise two main concerns: first, how to select the most suitable OTFT platform for a specific application and, second, how to estimate its potential in organic analog and digital circuits. In comparison to the silicon manufacturing wherever public models are soundly clear and generally cast-off to deliver designers with a comparative worthy explanation of any process, organic devices are yet missing for their whole device models that can completely label their electrical features. Many studies exist in the literature to understand the physics of these devices in order to mathematically describe their behaviors as discussed in refs.[14,15] and references there in. As need to understand basic device operation, to optimize device structures, and to consider novel device structures grows, the importance of numerical device simulation and modeling is rising as well. For numerical simulation and modeling commercially available device simulators are being exploited to investigate the specific devices as in ref. [1-54] and references therein. With organic semiconductors research efforts world-wide have focused on material synthesis and processing. Our efforts will focus instead on Characterization, Design and Device Modeling. The main objectives of this project are given below:

• Design of OTFT devices using physical TCAD modelling.

• OTFT spice modelling and parameter extraction.

• Measurements and modelling of device reliability and aging effects.

• The focus is on display device (OLED) drivers as these will be the first large scale organic semiconductor products.

• Application of the model in analogue and digital circuit simulo
Objective:

• In this work, we will perform numerical simulation of Organic Thin film transistors (e.g. Pentacene, DNTT, P3HT-based OTFTs etc) using commercially available device simulator ATLAS from Silvaco Inc.

• In simulation of OTFTs, we will use the concept of density-of-defect states (DOS) in organic thin film transistors.

• We will present a model of the OTFTs based on the tail and the deep states, which can produce well the characteristics of the OTFTs in both the subthreshold and the above-threshold regions.

• Fabrication, measurement and characterization of organic thin film transistors (OTFTs).

• Physics based compact model development of OTFTs for circuit simulation.

• Effect of dielectrics on the performance of OTFTs would be investigated.

• OTFT spice model parameter extraction.

• Measurements and modelling of device reliability and aging effects.

• The focus is on display device (OLED) drivers as these will be the first large scale organic semiconductor products.

• Model verification by application of the developed compact model in various analog and circuit simulation

Keywords: OTFTs, Fabrication, Compact modeling, Physical simulation

Expected Output and Outcome of the proposal:

We propose to develop compact model for OTFTs (pentacene based OTFT, P3HT based OTFT, DNTT based OTFT etc.) on flexible transparent substrates. Developed compact model will be very useful for circuit design and simulation using organic thin film transistors which can be used in display industry and other analog and digital applications. The developed compact models coded in Verilog-A language can be directly used in standard EDA tools for product design by semiconductor industry and research community for further investigation and evaluation of performance of integrated circuits. Also outcome of this project would be completion of Ph. D. thesis of one student and other M. Tech and Ph. D. students would also be benefited.

Time Schedule of activities giving milestones through BAR diagram.
Procurement of computers, hardware, software and installation of related hardware and software tools, literature review and numerical simulation of flexible OTFTs.

Fabrication, measurement and physical modeling of organic thin film transistors (OTFTs). Mainly bottom gate top contact OTFTs will be fabricated and numerically simulated. Effect of dielectric on performance of the OTFTs would be investigated.

Characterization of the devices would be performed. Also compact will be developed and comparison of the modeling results with measured results would be done.

Developed compact model will be applied to various circuit design applications for model validation e.g. PMOS inverter circuit design would be performed and same will be used in ring oscillator, Hybrid inverter, Hybrid operational amplifier and other analog and digital circuit design.
## Full Summary (in Rs.)

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<thead>
<tr>
<th>Institute</th>
<th>Manpower Budget</th>
<th>Consumables</th>
<th>Travel</th>
<th>Equipment</th>
<th>Contingencies</th>
<th>Other Costs</th>
<th>Overhead Costs</th>
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## Equipment Cost Detail:

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<th>Foreign Exchange Rate</th>
<th>Spare time for other users (in %)</th>
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Endorsement Certificate from the Host Institute

Project Title: Numerical Simulation and Compact modeling of Organic Thin Film Transistors (OTFTs) for Future Flexible Electronics

This is to certify that:
I. The applicant, Dr. Arun Dev Dhar Dwivedi, is working as a regular Professor, in the Department of Electronics and Communication Engineering, Poornima University, Jaipur (Raj.) (designation) in this institute since 14-12-2015 (Date).

II. The applicant, Dr. Arun Dev Dhar Dwivedi, will assume full responsibility for implementing the project.

III. The date of commencement of the Award starts from the date on which the University/Institute receives the bank draft/cheque from the Science & Engineering Research Board (SERB).

IV. The grant-in-aid by the Science & Engineering Research Board (SERB) will be used to meet the expenditure on the project and for the period for which the project has been sanctioned as indicated in the sanction letter/order.

V. No administrative or other liability will be attached to the Science & Engineering Research Board (SERB) at the end of the Research Award.

VI. The University/Institute will provide basic infrastructure and other required facilities to the investigator for undertaking the research objectives.

VII. The University/Institute will take into its books all assets received under this sanction and its disposal would be at the discretion of Science & Engineering Research Board (SERB).

VIII. University/Institute assume to undertake the financial and other management responsibilities of the project.

IX. The University/Institute shall settle the financial accounts to the SERB as per the prescribed guidelines within three months from the date of termination of the Research Award.

Dated: 24/1/17

Signature of the Registrar of University/Head of Institute

Seal of the Institution
• Progress Report of Research Project- Numerical Simulation and Compact Modeling of Organic Thin Film Transistors (OTFTs)-

Objectives:

1. In this work, we will perform numerical simulation of Organic Thin film transistors (e.g. Pentacene, DNTT, P3HT-based OTFTs etc) using commercially available device simulator ATLAS from Silvaco Inc.
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3. We will present a model of the OTFTs based on the tail and the deep states, which can produce well the characteristics of the OTFTs in both the subthreshold and the above-threshold regions.
4. Fabrication, measurement and characterization of organic thin film transistors (OTFTs).
5. Physics based compact model development of OTFTs for circuit simulation.
6. Effect of dielectrics on the performance of OTFTs would be investigated.
7. OTFT spice model parameter extraction.
8. Measurements and modelling of device reliability and aging effects.
9. The focus is on display device (OLED) drivers as these will be the first large scale organic semiconductor products.
10. Model verification by application of the developed compact model in various analog and circuit simulation
### Objective Wise Status of Project Work as on 26-12-2019

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<th>S. No.</th>
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<th>Publications/Patent* (No.)</th>
<th>Expected Month of Completion</th>
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### Published Papers


- **Ph.D. Scholar (Under Relevant Area of Research)**

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<th>Topic of Research</th>
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<th>Date of Registration</th>
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<tbody>
<tr>
<td>Shubham Dadhich</td>
<td>&quot;Numerical simulation &amp; Compact modelling of organic Thin Film Transistor (OTFTs).&quot;</td>
<td>Dr. Arun Dev Dhar Dwivedi</td>
<td>29.07.2019</td>
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<tr>
<td>Mahima Asthana</td>
<td>&quot;Investigation on Doped and Un-doped ZnO based Thin Film Transistors for Flexible Electronic Applications.&quot;</td>
<td>Dr. Arun Dev Dhar Dwivedi</td>
<td>09.08.2017</td>
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