FDP ON CMOS Analog Integrated Circuit Design

An intensive one-week training programme on "CMOS Analog Integrated circuit Design" was being organized for faculty of engineering and technological institutions by MNIT Jaipur. The objective was to provide an exposure to the participants to the state-of-the-art in CMOS Analog IC Design and hands-on training on Cadence Software.

Cadence Software.

Course Outcomes *Participants are expected to understand*	**Analog Design flow and Tool Leaning**
Concept Illustration on common mode signal, virtual short, virtual ground and single stage amplifier design	Analog design flow using standard PDK in Cadence software
Design issue and challenges in analog ICs	Using SCL's PDK, layout, DRC, LVS, PEX and GDS Tape-out
Design and simulation of single stage, differential amplifiers and different current mirror circuits	Introduction about SCL FAB and Fabrication Process Flow
Performance Analysis of Two stage OPAMP design with and without miller compensation	Illustration about wafer, device Test/ Packaging /QA Flow

Invited Experts – Dr. Shouri Chatterjee, IIT Delhi, Dr. Sougata Kumar Kar, NIT Rourkela, Sh HS Jatana, Svci/Engr „G", Sh Ashutosh Yadav, Sci/Engr „D", Sh Rajesh Srivastava, Sci/Engr, SCL Chandigarh and Experts from Entuple Technologies Pvt. Ltd, Bangalore

Dr Arun Dev Dhar Dwivedi

Professor

Department of EEE, PU


Academy Training Programme
on
CMOS Analog Integrated Circuit Design