Poornima University Jaipur

Department of Electrical and Electronics Engineering

Address: Plot No. IS-2027-2031, Ramchandrapura, P.O. Vidhani Vatika, Sitapura, Extension, Jaipur, Rajasthan 303905

(Second Advertisement)

Dated: October 13, 2017

Advertisement for the post of JRF under SERB DST sponsored project

Applications are invited for the post of Junior Research Fellow (JRF) in the Research Project entitled **"Numerical Simulation and Compact Modelling of Organic Thin Film Transistors (OTFTs) for Future Flexible Electronics" sponsored by Science and Research Board (SERB), Department of Science and Technology (DST)** Govt. of India for 3 years in the Department of Electrical and Electronics Engineering.

Qualifications: M. Tech. (VLSI/Microelectronics or ECE field)/M. Sc. Electronics/ M. Sc. Physics with specialization in Electronics or B.E./B. Tech/ (in ECE/Computer or related field) with minimum 55% marks from a recognized University.. Preference will be given to the candidates with First class M. Tech in Electronics (Microelectronics or VLSI design) or related field with exposure in relevant field. It is desired that the candidates possess experience in the area of numerical simulation and modelling of organic thin film transistors (OTFTs). NET/GATE qualified candidates are encouraged to apply.

Scope of Project: The project details include Numerical Simulation of OTFTs using Technology Computer Aided Design (TCAD) tools, Compact Model development of OTFTs using Verilog-A, device fabrication, characterization and validation of the proposed model.

Duration: The post is purely temporary on contract basis with an initial appointment for a period of one year (likely to be extended on yearly basis for a period of 2 more years or project duration whichever is earlier on periodic performance appraisal).

Fellowship: The fellowship is Rs.25000 per month for the first two years. It may be enhanced to Rs 28000 per month in third year after evaluating the performance as per norms. Further 20 % HRA can be sanctioned subject to approval from DST for this project.

How to apply: Interested candidates should submit their applications along with self attested photocopy of relevant documents in the prescribed format (Enclosure I) through email/post latest by **11 December 2017 (Monday)** as per instructions given at www.poornima.edu.in. **Only those candidates need to apply who are committed to work, and are ready to work for the entire duration of the project**. The application may be posted to the following address:

Interview: Eligible candidates can appear for the interview scheduled on 18 December 2017 (Monday) at 11 am in Admin II block of Poornima University provided they have submitted the application and documents at least through mail as above.

Postal Address:

Dr. Arun Dev Dhar Dwivedi
(Principal Investigator)
Professor, Department of Electrical and Electronics Engineering
Poornima University Jaipur

Plot No. IS-2027-2031, Ramchandrapura, P.O. Vidhani Vatika, Sitapura, Extension, Jaipur, Rajasthan
Jaipur – 303905

E-mail: adddwivedi@gmail.com, arun.dwivedi@poornima.edu.in

Phone No: +91 9450547267

Candidates should note the following points:

1. Selection committee of Poornima University Jaipur reserves the right to fix suitable criteria for short listing of eligible candidates.
2. Candidates will be short listed for the interview based on merit and experience of the available candidates. Decision of selection committee will be final. The date and time of interview will be informed by email to candidates and hence a valid email id should be provided by the candidate in the application.
3. No TA/DA will be provided to the candidates called for the interview.
4. The selected candidates are expected to take admission in PhD program of the Poornima University.
5. Canvassing in any form will disqualify the candidate from the eligibility.

Note:

1. Postal envelope should be clearly marked with "**Application for JRF under SERB Project"**
2. Email Subject should contain "**Application for JRF under SERB Project**" should be typed in Subject of email.
3. Application form must be in the format prescribed, no other format will be entertained.
4. You can attach additional pages/brief CV if needed, but simply sending CV without the filled application from may lead to disqualification.

Encl: Enclosure –I

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Application for the post of JRF in SERB Project

For Office Use Only

Serial Number: **Received on Date:**

Eligible: Yes/No **Called for Interview: Yes/No**

Paste recent passport size photo

1. Name: …….. 2. Date of Birth: ……

3. Father's Name: ……... 4. Email: ……

5. Contact Information:

(i) Telephone (with STD Code): ……..…….(ii) Mobile: ……..….

(iii) Address for Communication: ……..

……..

6. Educational Qualifications:

Class	Subject/Branch	Board/University	Name of School/Institute	Marks Scored (%/CGPA)	Year
10^{th}					
12^{th}					
B. Sc/B.E./B. Tech					
M.E./M. Tech/ M. Sc.					
NET/GATE					
Other					

7. Total Experience (in months) :…….

Organization	Designation	Duration	Responsibilities

8. Familiarity with (mention):

Silvaco/ Sentaurus/ Comsol/ Matlab/Verilog-A	
Fabrication/Characterization Techniques	
Other (……..)	

9. Publications (if any): (Please attach a separate sheet for publication details)

Publications	Journals	International Conferences	National Conferences
Mention Numbers (Only)			

I have provided correct information as above and I understand that, if found incorrect, I may be disallowed to appear in Interview/Test.

Signature of applicant with name and date

Note:

1. Attested Photocopy of all qualification and experience related documents needs to be attached.
2. Original Certificate(s) with one photocopy of each (duly attested) to be brought at time of Interview.
3. Date of interview shall be communicated via email after scrutiny.